General Digital Layout Considerations

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It is of course commonly agreed among electrical designers that signal integrity is good, and susceptibility and unintended emissions are bad! The layout designer will be tasked with keeping these in check.

Below is a list of things a designer should keep in mind while laying out their board.

Stackup

The importance of a good PCB stackup on reducing emissions and susceptibility as well as even improving signal integrity cannot be understated. The principles used when creating a good stackup can also be extrapolated to explain almost all good design decisions that the designer will make when subsequently laying out the board. For this reason, introducing the board stackup first will provide a good list of fundamental design principles to keep in mind for later.

There are many valid stackups that a designer could make work, but this guide will look at a 6 layer stackup that will work well when dealing with higher frequency boards (with signals up to a few 100s of MHz) and can be easily expanded to more layers. That stackup is as follows:

- Top: First Vcc voltage (ie. 3v3)
- Inner 1: GND
- Inner 2: First Vcc voltage (ie. 3v3)
- *Dielectric core* - non copper layer
- Inner 3: Second Vcc voltage (ie. 1v8)
- Inner 4: GND
- Bottom: Second Vcc voltage (ie. 1v8)

There are a few points to note that make this particular stackup very useful:

1. Both the power planes and the GND have duplicate layers. With good via stitching distributed around the board, this double layering allows the designer to run tracks without worrying too much about splitting planes in half. If current needs to get from one side of a long trace across to the other side, it can cross over it or under it by jumping to the other layer. This reduces power path lengths and current loops and does so with minimal effort from the designer.

2. Planar capacitance is maximized. Capacitance increases with a decrease in parallel plate separation distance. The designer must remember that a dielectric core will be thicker than pre-preg separation between copper layers. Using this knowledge, this stackup places the core sandwiched between two power-ground-power layer groups so that the power planes can enjoy maximum planer capacitance to their nearby dedicated ground plane. The thick core in the middle will not provide much capacitive coupling between the top 3 and bottom 3 layer groups.

3. Matching power planes are referenced to one dedicated ground plane, meaning a return current won't be inclined to move from one ground plane to another as it shadows the path taken by the signal. This shadowing is the concept of high frequency currents wanting to take the path of least impedance by returning as close to the initial signal path as possible - naturally minimizing the current loop where possible.

4. Power planes are on the same layer as the ICs. The designer will be able to easily provide a low impedance connection between the power plane and the Vcc pin of an IC by connecting directly to the plane rather than through a via which would introduce more inductance.
5. More dedicated power and ground layers means the electrical signal is given freedom to take a more desirable path, which reduces current loop area and allows circuits less impeded access to the nice planar capacitance mentioned above. Some caution here, though: too many layers can get confusing to keep track of and design errors could become harder to detect.

Modern digital electronics regularly deal with high frequencies and often strict EMC requirements, and a good or bad PCB stackup can make or break a design - often regardless of how well you adhere to other good design rules.

In the following sections, this guide will cover why these stackup characteristics are desirable, and how the designer might proceed in laying out a board that best continues to use the same core philosophies that went into creating the stackup.

Loops

Loops can impact signal integrity, cause unwanted emissions, and increase susceptibility of a circuit. Magnetic fields are the concern when talking about unwanted loops.

Inductance does exist along straight wires, though it is greatly increased by creating many loops or windings to concentrate the induced magnetic field. It can also be increased by increasing the area of a loop or winding. In PCB layout, the total path taken by currents from power to ground will always create a loop with some area, and as a result there will always be some inductance inherent to that pathway.

The formula for calculating inductance of a circular loop can

be quite complicated depending on how it takes into account non-idealities such as the skin effect, but the main lesson that can be taken away from it is that *inductance is directly proportional to the circle's radius*.

Inductance is useful for getting a sense of how a wide loop might add impedance for high frequency currents, but when thinking about susceptibility of a loop, thinking about the relation between the magnetic field and loop current might be more useful.

Again simplifying the example to be a perfect circle, the magnetic field at the center of a current loop is given as:

$$B = \frac{\mu_o * I}{2r}$$

Holding the current (I) constant, an increased loop radius (denoted as r, which relates to loop area) will increase the magnetic field. Adding in more factors: if the produced magnetic field is changing, then it has the ability to induce a current on a nearby conductor. Conversely an external changing magnetic field will have the ability to induce a current on the loop, with increased effect as the loop area increases.

This example can be useful for a designer to imagine both how an unwanted magnetic field might be produced by a signal loop, but also how an external magnetic field might easily couple onto an open loop.

Golden Rule

With an appreciation for the impact of current loops, the best question a layout designer can ask themselves is: *What is the full path that the current will be taking, and what frequency components might be involved at the various sections?*. This question can apply to power and signals, but also to unwelcome noise.

Path of Least Impedance

DC current will take the path of least resistance, but AC - and especially high frequency AC - will take the path of least *impedance*.

Knowing that a wide current loop will appear as a high impedance to high frequency currents and discrete capacitors and planar capacitance will appear as low impedance, it becomes clear how paths of lowest resistance might not always be the path that high frequency currents take.

An interesting thought is to consider a square wave signal. If the path of least impedance is not the same as the path of least impedance, the high frequency component currents during the rising and falling edge of the waveform will take a different path than the DC current during the steady states.

Note #3 of the stackup considerations, which puts the single ground plane between the pair of power planes, is related to trying to reduce the path of least impedance. Consider an example where in the above stackup the top and bottom layers were swapped. Via stitching would still connect the 3v3 planes together, but when high frequency current transitions from one layer to the other, the return current will not be able to shadow closely to the signal after going through the via unless there has also been ground stitching placed close to signal/power via.

Using Planar Capacitance

Every capacitor has a frequency response - that is to say that capacitors will act differently at different frequencies. If you consider a physically large through-hole capacitor, it will allow lower frequency AC currents through very easily (with some dependency on capacitance value). For high frequency currents, moving so far away from the ground plane and the added path length of the long leads will cause the capacitor to appear as a much higher impedance. High frequency current will not readily go through the physically

large capacitor.

The distributed capacitance created by placing a power plane very close to a ground plane will perform very well at higher frequencies. The designer might understandably think that the small capacitance that they've created (maybe 10pF - 1nF) between the planes will be negligible - especially in comparison to the many bypass capacitors that the schematic designer has no doubt littered through the schematic. It is the frequency response of this planar capacitance that makes it special.

A capacitor only performs well up to frequencies where the parasitic inductance intrinsic to it's physical structure becomes too great to ignore (inductive impedance is a function of frequency). Planar capacitance is effectively available at all parts of the board, and high frequency current could easily pass from power to ground at any point. When compared to a discrete bypass capacitor, it means the high frequency current on a plane doesn't need to travel to where the discrete capacitor is located on the board in order to pass to ground. In the case described, this current is probably unwanted transients or oscillations that the designer wants to shunt away from the power plane.

Conversely, this also means that circuitry that requires a sudden inrush of current will be able to pull from the distributed planar capacitance for the highest frequency components of the inrush rather than pulling from a discrete bypass capacitor which may not be very close-by. Even if a bypass capacitor were close-by, the more "strict" pathway that the current must take will almost always involve more inductance than compared to current coming from the plane which can come from every direction simultaneously.

To summarize, planar capacitance is effectively the lowest inductance capacitor the designer has access to, which allows you to sink and source the highest frequency currents (whether they are signal or noise).

Decoupling Capacitors

As mentioned above, planar capacitance is good for dealing with the highest frequency currents, but discrete decoupling capacitors also have huge value in a design. They provide much more capacitance, though at the cost of higher parasitic inductance. For this reason, it's useful for the higher amplitude and slightly lower frequency currents (though still good up to very high frequencies when used correctly).

From the perspective of an IC, it is concerned by two problems on it's power line:

- Voltage variation (from the supply itself or line modulation due to other ICs and their varied current requirements)
- Impedance which inhibits sourcing the high frequency components of its output signal.

In lower frequencies and higher amplitudes than those discussed with planar capacitance, bypass capacitors can help with the two power line problems.

The capacitors can act as filters on the power line, shunting noise away to ground before it can cause problems.

Simultaneously, they can act as low impedance reservoirs for the ICs while they are actively switching and present as a quickly varying load to the supply line.

The name of the capacitors (decoupling) describes their use to "decouple" the load from the power supply for some AC components.

Decoupling capacitors should be placed such that there is minimal inductance between them and the ICs they help. If there are no solid ground and power planes, then the capacitor should be placed very close to the IC. If, however the design does have dedicated ground and power planes, then the distance to the IC is less important as the plane provides a distributed low impedance connection. The goal at that point is to connect the capacitor as directly to those planes

as possible (using short traces to an immediate via connection) – though keeping the capacitor in the general area of the IC will of course still help to reduce the impedances between it and the IC.

While physical package size and the resulting parasitic series inductance is one non-ideality to keep in mind with decoupling capacitors, series resistance is also always a concern. For this reason, MLCCs (multilayer ceramic capacitors) are the best choice for decoupling capacitors due to their very low series resistance (ESR).

Coupling

A common tendency with PCB layout is for the designer to run signals close along-side eachother. It looks good and often saves space. The problem, though, is that this can easily lead to signals near-field coupling between adjacent lines, which can cause glitches and noise on otherwise clean lines.

This effect can be seen most dramatically on a line with high impedance termination beside something like a fast clock. Every clock edge creates a quickly changing electric field along the length of the clock line, which could easily induce a momentary voltage potential along the adjacent line. With the high impedance termination of the adjacent line, the voltage difference can build higher, and possibly appear as a real signal edge to the load.

Having the ground return plane directly underneath both these lines can help reduce the apparent electric field. As the clock edge creates an electric field, the ground return will produce the opposite electric field and the two can mostly cancel out.

With this strategy coupling can be reduced, though to further reduce coupling there will still need to be some minimum spacing between lines.

As a warning, some “differential” data lines can be commonly labeled as something like *DATA+* and *DATA-*, and they can appear as though the positive line will use the negative line as the return. The designer would then reasonably place those two lines close together in order to reduce loops and cancel out the near field. The problem is that these “differential” lines do not actually have differential current flow and will both individually have a ground return. From an electrical perspective, these are just two single ended data lines. True differential data lines do exist (like RS485), though paired single ended data lines can often look similar (like D+ and D- in USB).

Loops vs Electric Field Cancellation

The two concepts may appear to be indistinguishable:

1. Reducing the area of a current loop to reduce magnetic fields.
2. Keeping signals close to their return paths for electric field cancellation.

Though they can often be simultaneously happening and solved with the same tactic, they are distinct problems.

Magnetic fields are most present in low impedance (higher current) lines and loads, while electric fields will dominate in higher impedance lines and loads where the voltage potential is not readily shorting out.

Consider a dipole antenna (rabbit ears antenna) which is a pair of antennas pulled apart to look like rabbit ears. It works by having a positive voltage go up one side and a negative go down the other. This creates an electric field, which when oscillated at a frequency of wavelength twice the width of the antenna array, will effectively radiate in the far field (as RF). If a person where to take the two antennas and bunch them together, the electric fields produced would mostly cancel out and the array would no longer effectively

radiate. This an example of electric field cancellation that is clearly distinct from current loop reduction.

As previously stated, electric fields will be produced along lines and loads of high impedance, and the two antennas can be thought of as a signal and return wire with a near infinite load in between.

Reflections and Transmission Lines

Just like ripples in water can reflect off a concrete wall and travel back the way they came, electrical signal edges can reflect off a change in impedance (increase or decrease) and propagate back up the wire. Just like any wave, reflections can cause constructive and destructive interference with the inbound signal, and can cause a signal to appear to jitter up and down and the reflection bounces back up and down the wire.

Though the main solution is to use appropriate signal *termination*, there are also aspects of the stackup and the planes around the signal track that can worsen or improve signal reflections.

The impedance instantaneously experienced by a signal edge as it travels along a track is called the characteristic impedance of the track. It is a combination both of the series inductance of the track and return path, as well as the parallel capacitance created between the parallel copper plates of the signal track and the ground return. As the signal edge travels down the track it must charge this track capacitance while also developing the magnetic field due to the track inductance. This appears to the signal as a continuous and distributed impedance. In most high frequency designs, 50 Ohms is used as the target characteristic impedance.

Reflections can occur at discontinuities in this characteristic impedance. That may be a sudden widening or narrowing of the track, or a gap in the ground reference.

The characteristic impedance of a track becomes more of a concern as the track becomes electrically long (of length greater than roughly 1/20 of the wavelengths of concern). For very short tracks, the characteristic impedance becomes less of a concern.

To give an example with rough numbers: Take a clock of 30MHz with CMOS output, let's assume the edge of the clock is around 50 times faster than the clock period which is a common rule of thumb (though maybe a little on the fast side). This means the edge could have frequency components centered around 1.5GHz! That frequency has a wavelength of 200mm in air, and 1/20 of that is only 10mm. The dielectric constant of air is 1 and FR4 of a PCB is around 4.5. That means that a track on the top of the board will propagate in both FR4 and air, and as a result will have a signal velocity somewhere between speed of light in air and $\frac{c}{\sqrt{4.5}}$ compared to being in just air (close to constant c). A signal on inner layers will more reliably be travelling only through FR4. Typically, to avoid having to deal with tuning the characteristic capacitance of the track, a designer will simply make the clock path length short enough that it doesn't matter.

When a designer is faced with creating a track that is electrically long and requires controlled impedance, that will be called a *transmission line*.

For lower frequencies, reflections can still occur. Characteristic impedance of the track becomes slightly less of a concern, but the source and load impedance (dominated by resistance) is the main focus. In a CMOS digital logic circuit, an output may be around 30 Ohms of source impedance while the load impedance could be much much higher depending on what is receiving the signal. An op amp input may appear as MOhms of impedance. Without treatment, reflections will occur; depending on the length of the track, unwanted fluctuations on the signal line will be produced and may cause false signal edges.

Much more can be said on termination and the many ways to

approach it – each with upsides and downsides. The optimal choice can depend on many factors and may take iterating and testing in order to determine.